Cadence Allegro and OrCAD: What’s New in Release 17.4-2019

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A new version of the Cadence Allegro and OrCAD products has been released, bringing several enhancements and new features.

### Topology Explorer
- New Signal Integrity User Experience Now Available

### OrCAD Capture and OrCAD Capture CIS
- Simplified Project Creation and Simulation Flow
- Streamlined Workspace
  - Application and Canvas (Schematic Page) Theme
  - Workspace Customization
  - Single-Point Access to Modeling Applications
  - Enhanced Search Pane
- Simplified and Improved PCB Design Flow
  - Online DRC
  - PCB Menu
  - New Layout Window
  - Design Sync
  - Design Sync Setup
- Accessing External Parts from Capture
- New Capture Start Page

### PSpice and PSpice Advanced Analysis
- Enhancements in PSpice Workspace
  - Application Theme
  - Streamlined Workspace
- New PSpice Models and Library
- PSpice Library Cleanup

### Help System
- Improved User Interface for Cadence Help
- Help Landing Page
- OrCAD Tutorial
This document describes the new features and enhancements in Cadence® OrCAD® and Allegro® products in release 17.4-2019 (also referred to as 17.4 in this document).

- **Allegro PCB Editor and Allegro Package Designer+** on page 2
- **Allegro ECAD-MCAD Library Creator** on page 23
- **Allegro EDM** on page 27
- **Allegro System Capture** on page 32
- **Topology Explorer** on page 49
- **OrCAD Capture and OrCAD Capture CIS** on page 50
- **PSpice and PSpice Advanced Analysis** on page 78
- **Help System** on page 88
This section describes the new features and enhancements in the Cadence® layout editors, Allegro® PCB Editor and Allegro® Package Designer+, in release 17.4-2019. If a feature is available in only one of the layout editors, a note is provided.

- **17.2 Database Compatibility Mode** on page 3
- **Symphony Team Design Option** on page 4
- **Hierarchical Route and Via Keepouts** on page 6
- **Allegro Constraint Complier** on page 7
- **IPC 2581 Spec Properties** on page 7
- **Mask Defined Pin Annular Ring Check** on page 8
- **Via Array Update** on page 10
- **Contour Routing Update** on page 13
- **Copy/Paste Update** on page 13
- **Via Structure Update** on page 14
- **3D Canvas Update** on page 16

To view the latest updates for hardware and software requirements, see Allegro Platform System Requirements. Also refer to Migration Guide for Allegro Platform Products, Product Version 17.4-2019.
17.2 Database Compatibility Mode

Using the 17.2 Compatibility feature, you can open a 16.6 or 17.2 database in release 17.4-2019 and work on it without saving it in the new 17.4 database format. You can make database changes but only those that are compatible with 17.2. Even if the Compatibility mode is enabled, a 17.4 design opened in the current release will remain in the 17.4 database format.

**Note:** Release 16.6 database opened in release 17.4-2019 will be saved in 17.2 format with this mode active.

Enable 17.2 Compatibility mode either by setting `database_compatibility_mode` from the User Preferences Editor under the **Drawing** category or by adding `database_compatibility_mode` with a value of 17.2 to the PCBENV/ENV file.

![User Preferences Editor](image)

When you open a release 17.2-2016 design in 17.4-2019, with the compatibility mode enabled, a dialog is displayed indicating that the mode is active. You can decide to either maintain the 17.2 database format or disable the mode to enable the new release (17.4-2019) features and save the design in the 17.4-2019 database format.

![Compatibility Mode Dialogs](image)
When a design is opened in the compatibility mode, the window title bar and the status bar display 17.2 Compatibility Mode. If you open a 17.2 design in 17.4, with the compatibility mode disabled, a dialog will be displayed indicating that the database will be updated to the current software version.

### Symphony Team Design Option

We continue to enhance the concurrent environment so that extended team members can engage in design activities throughout the design cycle. You can now connect to a Symphony session using an Allegro® Physical Viewer Plus product license to review and mark up the design actively being worked on and not a stale copy.

Symphony Team Design Option availability:

- **Allegro PCB Designer and Allegro Venture PCB Designer**
  - PCB design, constraint management, in-circuit testing and manufacturing verification, signal integrity (SI) analysis screening

- **Allegro Physical Viewer Plus**
  - Full viewer functionality with mark-up capabilities. (Mechanical, Regulatory, Manufacturing Engineering reviews)

- **Allegro Package Designer+**
  - IC/Packaging design support

- **Allegro Sigrity SI**
  - Real-time analysis of active database as work is completed
  - Exchange of advanced signal integrity results with PCB Designer

**Release of Constraint Edit Mode:**

- Environment variable no longer required to access functionality
- Allows a client Constraint Manager access while everyone continues their concurrent design work
Constraint modifications across all domains with full hierarchical support (Net Class, Differential Pairs, and so on)

17.2 Compatibility Mode:

- Support of new compatibility mode, which maintains release 17.2-2016 database format
- Verification when joining a session to ensure client is in compatibility mode when the server is in compatibility mode

Note: This new mode does not allow release 17.2 clients to connect to a 17.4 Symphony Server but prevents the update of 17.2 database to the 17.4 format.
Hierarchical Route and Via Keepouts

You can now define keepout by layer type and location using the additional Route and Via Keepout subclasses that have been added to Symbol Editor. Following a model similar to Constraint Regions, use the OUTER_LAYERS, INNER_SIGNAL_LAYERS, and INNER_PLANE_LAYERS subclasses to create keepout shapes.

These new subclasses are only available for assignment in Symbol Editor and any shape geometries you create are replicated to the appropriate subclasses when you place a symbol. These auto-generated keepouts are similar to other keepouts in a design but you can update them only in Symbol Editor.
**Allegro Constraint Compiler**

Various manufacturers provide EDA design guidelines to ensure customers leverage technology to its fullest extent and develop products that perform as expected. These design guidelines are normally interface specific, and the designers interpret the guidelines to apply appropriate rules in layout tools. Often, these rules are not necessarily understood and that leads to under- or over-constraining of a design. Manufacturers sometimes provide reference designs and design review services to help customers achieve the best results for their products, but this can increase the design schedule considerably, which could impact the overall product schedule.

The 17.4-2019 release introduces Allegro® Constraint Compiler (ACC), an infrastructure to support automatic translation of design constraints from an external source directly into Constraint Manager. ACC is not meant to be a Constraint Manager replacement but a mechanism to inject constraints, at the interface level, based on manufacturer guidelines. ACC is used to seed initial constraint information in a design or update a design that has existing constraints. At the simplest level, ACC uses the connectivity (Buses, Differential Pairs, Nets, and so on) of a design in conjunction with “data agnostic” constraint information to create specific rules for various interfaces in a design.

**Benefits of the Allegro Constraint Compiler**

- Ensures consistent constraint entry because of a single-source reuse path from design to design
- Facilitates the automatic generation of constraint containers (Differential Pairs, Net Classes, Net Groups Match Groups, and expanded Constraint Rule Sets)
- Avoids manual effort by using *one-to-many* constraint explosion to propagate rules down to the lowest level, generating all supporting objects and groups

**IPC 2581 Spec Properties**

IPC-2581 is an XML-formatted manufacturing data file, which contains information required to fabricate, assemble, and test a Printed Circuit Board (PCB). The IPC-2581 format allows the inclusion of descriptive details that may be attached to specific objects, such as assembly instructions and/or fabrication notes typically displayed within a Fabrication or Assembly drawing. The instructions (or note call-outs) are defined as a specification or, in IPC-2581 terms, a SPEC. SPECs are included as attachments to components or as general design data that may be used by post-design processes.
**SPEC** is an XML element within the IPC-2581 data that is identified by a name (say, **FAB NOTES**) and contains one or more items that make up the **SPEC** definition. In the **FAB NOTES** example, the traditional method is to add a note to a fabrication drawing and create an image layer or document file (each note item). This requires the drawing or document to be opened to find and view the fabrication notes.

By defining a **SPEC** that is composed of the fabrication notes, the notes become part of the IPC-2581 data and are directly read by an IPC-2581 viewing tool, reducing the need to locate the correct drawing or document to read the notes.

Another example would be to define assembly notes for a heat sink to be added to a part. The assembly note might instruct users to add a specific thermal epoxy first, then add the heatsink after the epoxy is applied.

In release 17.4-2019 of Allegro®/OrCAD® PCB Editor and Allegro Package Designer+ (APD+), you can define **SPEC** elements and apply them to a board drawing, a component, or specific elements. After creating a **SPEC**, you can export it to a **SPEC** template that can be imported by other designs.

**Mask Defined Pin Annular Ring Check**

A new **Mask Defined Pad** check has been added to the Design for Manufacturing Annular Ring checks and the DesignTrue DFM Wizard template file. There are two common types of padstack definitions when it comes to soldermask to pin pad size ratios. The first, metal-defined padstack (sometimes referred to as non-mask defined padstack), is where the solder mask opening is typically larger than the pin pad. The other is a mask-defined padstack, where the solder mask size is typically smaller than the pin pad. The mask-defined pad is often used for BGA components to contain the solder ball within the pin pad and prevent outflow of solder.
In the case of BGA pins, the mask opening must have an annular ring of a recommended size. The annular ring check verifies that the mask size is smaller than the pin pad, but is not too small an opening. The rule measures the annular ring of the mask inside the pin pad.

A DRC is displayed if the soldermask size is equal to or greater than the pad size, and if the soldermask size annular ring is greater than the annular ring size specified. Not all pad definitions in a BGA or in a design require mask-defined pads. Component pins that require mask-defined pad stacks are identified by adding the `Mask_DEFINED_Pin_Type` property.
Via Array Update

An array is an arrangement of similar objects. For a PCB and package substrate, arrays are generally rows or columns of vias or structures attached to a net, near or inside other objects. New for the 17.4-2019 release is the addition of a singular array command for adding, updating, and deleting many different array types. On screen dynamics provide you control and feedback by letting you dynamically adjust arrays before placing them. Newly added visuals and graphics make arrays easy to understand letting you get what you want the first time.

Use the Via Array command to add both vias or structures in various patterns to the designs. You can easily choose the starting point, location, and geometry of the array ( spacings between objects). Use the existing legacy controls to preview, adhere to DRCs, and extend a selection to include all objects of a net. The previously termed boundary and matrix arrays are combined into one command for ease of use with the following array types being available:
Boundary Arrays

- Single Sided – Add an array along one side of one or more selected objects.
- Both Sides – Add an array to both sides of one or more selected objects.
- Centered – Add an array centered on one or more selected objects.
- Between – Add an array between all selected objects. Objects must be parallel.
- Surrounding – Add an object surrounding the selected objects.
- Radial – Add a circular or radial pattern of vias or structures around one or more selected objects

Matrix Arrays

- Across Board – A matrix of vias or structures is added filling the board outline.
- Across Shape – Matrices are added filling one or more selected shapes.
- Across Windowed Area – A matrix of vias or structures is added to a windowed area.
Each array type comes with its own unique graphics to help explain the functionality. Swapping between the array types toggle all appropriate settings, name, and graphics to match.
Contour Routing Update

The 17.4-2019 release now supports the previous Enhanced Contour behavior as the default contouring method. In addition to the previously supported functionality of latching/unlatching and shoving, this release focuses on ease of use and power by adding additional spacing controls and full constraint region support.

Precisely and quickly follow complicated geometries with their routes using the Contour functionality, available within the Add Connect command. Now, dynamically lock onto existing elements in order to follow them. Commonly suggested uses of this technology include flex and bus routing due to their predictable paths.

Copy/Paste Update

In previous versions of layout editors, copying of objects was performed by selecting objects and pasting them to one location at a time. While the use model was simple, the functionality was limited. The 17.4-2019 release aligns the copying functionality of the layout editors with other popular software applications by adding familiar behaviors. This new copy command combines the precision of single click or single location pasting with the power of window select or multi-location pasting. As with most applications, copied objects are buffered for pasting at a later time. You can paste the last copied object at any time simply by using the paste command.

Copy

The Copy command now adds the selected objects to a buffer and automatically starts the Paste command to enable the placing of objects on the canvas.

Paste

The Paste command supports all legacy “copy” options as well as new support for shape net retention. In addition to these options, pasting can be used in two different manners.

- Single Location Pasting
  - Copying of objects and pasting at one location per click
  - Object snaps to the singular selected object or location

- Multiple Location Pasting
  - Copying of objects and pasting at multiple locations through window select
Objects snap to all selected objects

Via Structure Update

New in the 17.4-2019 release is a single unified Create Structure form. This form combines the previous Standard, High Speed, and L-Comp forms into one easy-to-use form while also adding descriptions and walkthrough guides for how each can be created. Graphics provide visual examples of each structure making it easier to identify possible use cases for each.

- **Structure Selector**: allows you to change the type of structure you want to create.
- **Description**: explains the structure type as well as provides instructions for creation.
- **Define/Generate**: provides the controls for generating and exporting the structures.
The Route – Structures – Create command supports creation of the following three different types of structures:

- **Standard Via Structure (SVS)**
  - Supported Objects – Traces and Vias
  - Connectivity Support – Objects can connect to up to one net
  - Export Format – eXML

- **High Speed Via Structure (HVS)**
  - Supported Objects – Traces, Vias, Static Shapes, Route Keepouts
  - Connectivity Support – Objects can connect to up to two nets (one primary, one return)
  - Export Format – eXML

- **Inductance Compensation Structure (L_Comp)**
  - Supported Objects – Traces and Route Keepouts
  - Connectivity Support – Objects can connect to up to one net
  - Export Format – eXML

Structures are flexible and adaptable. If any piece of etch or circuit is to be re-used multiple times, structures provide a fast way of adding, refreshing, and replacing them without having to do so one at a time. Examples of use include but are not limited to the following:

- Antennas
- Coils
- High-speed “launches”
- HDI structures
- BGA pin escapes
- RF Structures
3D Canvas Update

3D Canvas continues to add significant features as well as fine tune existing features. With features under continual development, this release covers incremental updates that will enhance user experience. The popular Cutting Plane feature has been improved with quick access from a pop-up and controls in the Options pane; mechanical symbols now have a global transparency setting option; non-STEP model Symbol Representation can use the existing Place_Bound shape or the newly added DFA_Bound shape; unplated holes in footprint (.dra) files are now visually represented; the z-direction position of STEP models can include the pastemask thickness if needed; and lastly, only the exterior layers and models can be sent to 3D Canvas via a new “skinning” user preference.
Usability Improvements Associated with Cutting Plane

The popular Cutting Plane feature is now easier to use. Invocation of it is now done through a context menu with the user-adjustable settings now located in the Options pane. The performance of this feature has also been greatly improved.
Mechanical Symbol Transparency

Designers who wish to “peek” inside a PCB assembly encased with a mechanical cover can now do so. Now look through the mechanical cover into an assembly by setting the global transparency/opaqueness setting (Setup – Preferences – Symbol Representations).

Before Release 17.4-2019

Release 17.4-2019
Symbol Representation Using DFA_Bound Shapes

When PCB designs are brought into 3D Canvas, if footprints do not have a STEP model mapped to it, 3D Canvas currently uses the Place_Bound shape as well the height property of the shape to create an extruded 3D representation. With the 17.4-2019 release, you can choose between using the existing Place_Bound shape or the newly added DFA_Bound shape.

Creating DFA_Bound shapes at MMC (Maxim Material Condition) allows you to do collision checks in 3D Canvas using the worst case scenarios between models. To use this new feature, set 3D_symbol_include_dfa_bound in Setup – User Preferences – Display – 3D. When you view a design in 3D Canvas, choose between DFA_Bound shape or Place_Bound shape in 3D Canvas by setting the options under Boundary Shape Source under Symbol Representation (Setup – Preferences).
Unplated Holes in Footprints

Unplated holes in footprint (.dra) files can now be visualized when the footprint is brought into 3D Canvas. Previously, unplated holes were not represented.
STEP Models and Pastemask

In some system designs, such as complicated telephony devices, even the most minuscule space is critical. With the 17.4-2019 release, the position of 3D models can now be globally adjusted to take the thickness of solderpaste into account in the “z” direction. By default, the STEP model location in the “z” direction is the bottom of the model located directly on top of the copper pads.

Set 3D_symbol_place_on_pastemask under Setup – User Preferences – Display for the model position in the “z” direction to take the thickness of the pastemask, defined in Cross-section Editor, into account.

Name of Design Now Listed on Top Header

The 3D Canvas top header line now indicates the name of the design loaded into view.

Outer Layers Only Mode

Limited memory and large file size may create problems in visualizing large designs in 3D Canvas. If you do not have sufficient memory, the types and size of designs capable of being
loaded into 3D Canvas can be limited. You can now use skinning along with some of the already existing options in getting large designs into 3D Canvas. Skinning is the loading of only the external components and layers in 3D Canvas. Set 3D_canvas_skinning under Setup – User Preferences – Display – 3D to turn on skinning.
Allegro ECAD-MCAD Library Creator

This section describes the following enhancements and new features in Allegro® ECAD-MCAD Library Creator in release 17.4-2019.

- **Allegro Settings Dialog** on page 24
- **Dimensions Styling** on page 24
- **Class/Subclass Mapping** on page 25
- **Padstack Export** on page 25
- **Miscellaneous Enhancements** on page 26
Allegro Settings Dialog

The Allegro Settings dialog is redesigned with separate Import and Export tabs.

For more information about the Import and Export tabs, refer to the Allegro Settings section of the Allegro Library Creator User Guide.

Dimensions Styling

With this version, dimensions can be added to a footprint as an aid in drafting, for measurements, and for documentation purposes. Library Creator supports both symmetric and relative dimensions. Horizontal, vertical, and diagonal dimensions of either type can be created using the 2D Toolbar.

Users can also:
- Control the formatting and styling of a dimension.
- Modify the settings for individual dimensions.
- Create custom dimension styles.
Export dimensions to Allegro PCB Editor.

For more information about adding dimensions, refer to the *Dimensions* section of the *Allegro Library Creator User Guide*.

Class/Subclass Mapping

The majority of the layers commonly used in Allegro package and mechanical symbols are predefined in Library Creator and mapped automatically to the applicable Allegro PCB Editor classes and subclasses. Now, it is possible to add additional layers using Layer Setup and map them to an Allegro PCB Editor class and subclass using the *Allegro Setup* dialog.

Padstack Export

Padstacks created by rules or interactive editing in Library Creator can be exported to Allegro PCB Editor using *File – Export – Allegro*.

For more information about exporting padstacks, refer to the *Padstack Export* section of the *Allegro Library Creator User Guide*. 
Miscellaneous Enhancements

- Library Creator can be installed using the standard OrCAD/Allegro 17.4 installer.
- Library Creator directly interacts with Allegro PCB Editor without using SKILL files. This speeds up the export of footprints to Allegro PCB Editor and also allows more information to be exported, such as dimensions.
- Users can enable or disable the reporting of variable values and rules triggered during rule execution using Tools – Preferences – Reporting.
This section describes the following enhancements in Allegro® EDM in release 17.4-2019.

- Pulse Platform on page 28
- Pulse Manager on page 28
- Release to PLM on page 29
- Support for TLS 1.2 for Client-Server Communication on page 31
What’s New in Allegro EDM 17.4-2019

This section describes the new features in Allegro EDM 17.4-2019.

Pulse Platform

Starting with this release, the desktop and server-based data platform of Allegro EDM is implemented in a microservice framework, referred to as Pulse. The framework provides services such as library management, the ability to search for parts, embedded data management, and enterprise PLM integration.

The architecture is designed to provide a secure ECAD product data management (PDM) platform, which enables easier data-driven decision making in the design process (also referred to as data-driven design). The user experience provided by the platform is designed to provide embedded functionality in authoring tools, such as Allegro System Capture, and a comfortable web-based experience for the engineering community. Further, the platform is designed to support cloud deployment enabling customers to securely manage their data in an on-premise data center or in the public cloud.

For details on configuring the Allegro EDM server and clients on the Pulse platform, refer to Allegro EDM Configuration Guide.

Pulse Manager

This release introduces Pulse Manager, a web-based administration console used to configure the Pulse platform. Easily accessed through a browser, Pulse Manager allows you to configure the Allegro EDM server and its clients, manage your logs, data, disk space quota, data backups, and various other tasks.
For details on configuring the Allegro EDM server and clients on the Pulse platform, refer to *Allegro EDM Configuration Guide*.

**Release to PLM**

The Release to PLM function enables users to easily publish design data, including the ECAD BOM and any manufacturing deliverables, to an enterprise’s PLM system or its manufacturing partners. Release to PLM provides a simple workflow enabling engineers to easily and consistently provide their design data to other business stakeholders as necessary.
For companies that are not using a supported PLM system, *Release to PLM can also easily be used to create a data repository within your file system.*

With tight integration between the enterprise PLM and the ECAD design environment, you can now easily publish the ECAD BOM structure to a PLM system, enabling earlier product collaboration and more data-driven strategic product decisions.

Release to PLM simplifies the interaction between Cadence front-end applications and PLM systems:

- Easily search for and locate what you need through familiar interfaces in the Cadence front-end applications, such as Allegro System Capture.
- Apply approved parts to your designs while keeping all metadata in sync.
- Provides a simple, three-step workflow, which helps you generate and publish the required ECAD content to PLM systems from within the ECAD tool itself.
Support for TLS 1.2 for Client-Server Communication

To continue to secure communication, privacy, and data integrity between the Allegro EDM server and its client servers, this release adds support for the industry-standard Transport Layer Security (TLS) 1.2 cryptographic protocol.
Allegro System Capture

This section describes the following enhancements and new features in Allegro® System Capture in release 17.4-2019.

- **User Interface Changes** on page 33
- **Enhancements for Object Selection and Replacement** on page 40
- **Extended Design Reuse Options** on page 43
- **Reporting Block Differences** on page 44
- **Preserve Locally Edited Hierarchical Block Symbols** on page 45
- **Custom XNet Pin Pairs Definition** on page 46
- **Improved Logging and Crash Handling** on page 46
- **Pulse Platform Integration** on page 47
User Interface Changes

One of the key focus areas of System Capture is the interface. Context-sensitive menu options and controls get displayed instead of a crowded screen where you need to figure out icons. Most related windows are floating and can be docked or pinned per your comfort. You can customize the placement and size of every window. Some of the key changes from earlier releases are in the display and configuration of:

- Project Viewer
- Properties Window
- Changed Windows Behavior
Project Viewer

You can view and access all elements of the project, from all blocks in the design hierarchy to each sheet’s thumbnail. All controls for showing the project elements, such as blocks, sheets, sheet numbers, and so on, are accessible from the Gear icon.

The following image shows you the project elements that you can include in the Project viewer window.
Properties Window

To see the properties of the selected objects on the canvas, choose View – Properties. You can modify the line colors, font colors, and set default styles for graphic objects. The properties for components are displayed in alphabetic order.

Changed Windows Behavior

Most of the drag-drop and dock features are intuitive and a quick exploring of the UI will reveal the changes in how the windows’ placement can now be controlled.
Dockable Library Search Results

The Library window can be moved to any monitor, in case you have multiple displays connected, or side of the canvas. To return the window back to its previous location, double-click its title bar. To lock the placement of the window, click the pin.
Hidden Windows show as Tabs

The following image shows how hidden windows are shown.

![Screenshot showing hidden windows as tabs]

Optimized Toolbar

Commonly used tasks are accessible from the central toolbar. Some of the toolbar buttons, expand when clicked to display more options.

Figure 2-1

![Screenshot showing expanded toolbar buttons]
Special Symbol Preview

You can see the previews of the symbols when choosing a special symbol for placing, or when adding a symbol.

Changes in Menus Shortcut Keys Behavior

To access the menu bar commands, press the Alt key. You will now see the shortcut letter for each menu. In the following image, you can see the letters for the default menus. The custom menus, however, do not have the letters specified.

If you press Alt + <Menu Letter>, such as Alt + F or Alt + T, you will notice that:
- The menu opens at the default cursor location

- The menu name is displayed for a few seconds on the canvas.
Enhancements for Object Selection and Replacement

Selection Filter

The selection filter helps you quickly select objects of specific types and also shows the count of objects selected.

Find and Replace

- The results of a Find operation are now displayed in separate tabs for each object type.
- In-place editing can be done for all modifiable properties and then used as replacements.

- Search results can now be edited externally and then used as replacements.

The summary of changes made is reported and you can review the changes in the log file.

**Replace Special Symbols**

Right-click any special symbol on the canvas and choose *Replace*.

Select another symbol and click *OK*. 
Replace Sheets Across Designs

Important

Currently available as a command-line feature only

The importSheets Tcl command has been enhanced and can now be used to replace sheets of a design with sheets from another project. This command can bring in sheets from both DE-HDL and System Capture projects. Multiple sheets can be replaced in a single operation.

Syntax

importSheets

srcProj <source project path>

lib <library name>

cell <cell name>

replacePages <page numbers>

type <source design type>

destBlockName <cell name>

preserveRefdes [0 | 1]

When specifying pages to replace:

- Ensure that the number of sheets are an exact match and are either individual sheets or a range.

  For example:

  - {1,3,5} -> {1,4,6}
    Here, three specific sheets are getting replaced.

  - {11-15, 2-4} -> {21-25, 14-16}
    Here, two sets of ranges are getting replaced. The number of pages in each range is an exact match.

  - {4, 6, 9-12, 14, 18-20} -> {12, 13, 14-17, 20, 22-24}
Notice that the order of the individual sheets and ranges is maintained. And the ranges have the exact same number of pages.

- You can preserve the Reference Designator of the pages.
- In case of any problem, the entire operation is canceled.

Extended Design Reuse Options

Create New Project from DE-HDL

You can now create new System Capture designs that are created from DE-HDL projects. The following are included in the System Capture project:

- Library data from the DE-HDL source
- Local libraries that are referenced in the DE-HDL project
- Project settings for Part Table Files, PPT option sets, and Custom Variables
- Information for relative paths
- DE-HDL design data

Additionally,

- Part information gets cached in System Capture
- Part Manager synchronizes design parts with the reference library
- Projects can be created without a site definition when using a DE-HDL archived design

Import Voltage from Constraint Manager

Voltage property assigned on power nets on the schematic or in Constraint Manager are now available in System Capture when importing DE-HDL designs as blocks or when importing schematic sheets.
Reporting Block Differences

A command-line utility is now available that compares logical connectivity between two designs, or two versions of the same design, and generates a list of netlist differences. The report classifies differences as:

- Connectivity objects
- Properties compared

**Note:** Non-electrical objects and constraints are *not* compared.

The differences reported are based on:

- Connectivity ID – compares revisions of a design
- Logical Name – compares two different designs

**Syntax**

```
logicalDesignCompare
   -dstproj <Destination Project Path>
   -srcproj <Source Project Path >
   -report <Differences Report Path>
   [-block <Block Name>]
   [-mode id | name]
   [-log <logfilepath>]
```
Preserve Locally Edited Hierarchical Block Symbols

You can now edit the symbol for a block created by another user after instantiating it in your design hierarchy. Some reasons why the symbol for a block might be changed are to modify the connectivity or improve readability.

After making changes to a local version of the symbol, when you re-import the updated block:

1. Logical changes will be imported
2. The locally modified symbol will not be overwritten

Here is how this is implemented:

1. Import a block as Read-Only.
2. Unlock the block symbol.
3. Make changes to the local symbol.
4. Re-import the block.

System Capture checks the locally modified symbol and prompts you to preserve or overwrite the local symbol.
Custom XNet Pin Pairs Definition

A new panel has been added to the Properties tab. It displays XNet pin pairs. You can also create XNet pin pairs by clicking on pins of a component.

The panel displays whether the XNet pin pairs are defined in the library or are defined on the schematic. Non-discrete components require library or instance definition. Using this pane, you can view or modify XNet pin pairs, and copy XNet definitions to other instances of the same type. To remove XNet pin pairs, use the reset options.

Improved Logging and Crash Handling

Event logging has been enhanced and all log files are stored in Pulse Data Mart, such as design status reports and command logs. In case of an unexpected tool exit, a zip file is created that contains diagnostic data.
Pulse Platform Integration

System Capture now comes with embedded data management, which is handled internally, and is transparent to the user. Data is controlled internally when the Save command is used. You can also optionally create **Commit Points**, which offers the following benefits:

- Simple branching support
- Easy rollback
- Preview any version without opening
The version tree is generated based on when the *Save* or *Commit* commands are clicked.
Topography Explorer

This section describes the all-new Cadence® Sigrity™ Topology Explorer available in release 17.4-2019.

- **New Signal Integrity User Experience Now Available**

**New Signal Integrity User Experience Now Available**

Release 17.4-2019 unites the user experience of Allegro® System Capture schematic environment with Sigrity™ SystemSI. This new user interface combines the Parallel Bus and Serial Link analysis capabilities, and offers AMI Builder to generate AMI models. In addition to improved usability, the following key features are available:

- Bus characterization enhancements
- JEDEC measurement and report enhancements
- Sweep Manager enhancements
- Block connection enhancements
- PCI Express Gen 5 compliance kit
- Custom compliance kit

**Note:** To be able to fully utilize the benefits of this new Signal Integrity User Experience, you will need to install both Cadence® OrCAD® and Allegro® 17.4-2019 and Sigrity™ 2019 base release.

For detailed information, see the following documents included in the OrCAD® and Allegro® 17.4-2019 Base release:

- **Topology Explorer User Guide**
- **Topology Explorer Frequently Asked Questions**
- **Topology Explorer Known Problems and Solutions**
OrCAD Capture and OrCAD Capture CIS

This section describes the following enhancements and new features in OrCAD® Capture and OrCAD® Capture CIS in release 17.4-2019.

- **Simplified Project Creation and Simulation Flow** on page 52
- **Streamlined Workspace** on page 53
  - Application and Canvas (Schematic Page) Theme
    - Well-Organized Toolbars
    - New Icons
  - Workspace Customization
    - Viewing Panes in Canvas Area
    - Customizing Panes
    - Multiple Monitor Support
    - Project Manager - Multiple projects in a single pane
    - Common Window for Component Placement
    - Common Window to Display Output
  - Single-Point Access to Modeling Applications
  - Enhanced Search Pane
- **Simplified and Improved PCB Design Flow** on page 68
  - Online DRC
  - PCB Menu
  - New Layout Window
  - Design Sync
  - Design Sync Setup
- **Accessing External Parts from Capture** on page 76
■ New Capture Start Page on page 77
Simplified Project Creation and Simulation Flow

The 17.4-2019 release introduces the concept of universal projects, which allows you to create a project without having to select a project type. Further, with the new user interface, you can create a project along with the option to enable PSpice simulation.

Select *Enable PSpice Simulation* if you want to start PSpice simulation.

Even if you do not select *Enable PSpice Simulation*, you can configure simulation settings and perform PSpice simulation any time during the design flow. The *PSpice Resources*
Streamlined Workspace

OrCAD Capture provides you with a large set of user-friendly tools and features to easily capture your schematic design. With the 17.4-2019 release, the workspace has been enhanced to ensure fast schematic design creation in an optimized manner.

Many new improvements have been done in the Capture workspace to ensure greater ease of use and a satisfactory user experience.
Application and Canvas (Schematic Page) Theme

In the 17.4-2019 release, Capture opens in a dark theme by default, as shown in the following figure. A dark theme reduces power usage, improves visibility, and makes it easier for screens to be read.
**Setting Application Theme**

You can set the theme from the *Preferences* dialog box for both the application and the canvas (schematic page).
Well-Organized Toolbars

Toolbars have been reorganized according to function, and the icons in these toolbars are arranged based on their menus. You can toggle individual icons on or off in the toolbar.

New Icons

With two new themes in 17.4-2019, Capture also introduces theme-specific icons.
Workspace Customization

Panes are now displayed consistently across all OrCAD applications. All resources opened from a project are displayed as horizontal *Tabbed Documents* in the canvas area.

By default, all panes displaying any kind of output are at the bottom of the application. If multiple panes are open in the output window, they are displayed as docked and tabbed panes.

Viewing Panes in Canvas Area

Open panes in the canvas area are displayed as horizontal pages called *Tabbed Documents*. These tabbed documents or pages, which have labels, do not get reduced in
size or resolution when the number of open pages increases. With this release, you can also move and arrange these pages according to your requirement.
Customizing Panes

You can drag and drop panes to move them in the workspace using the docking markers as shown in the following figure.
Alternatively, you can use the pop-up menu options for each pane, such as *Floating, Docking, and Tabbed Document.*
Multiple Monitor Support

You can drag a tabbed document and display it on another monitor as shown in the following figure. In this example, the active project has been dragged and becomes a separate window, which can be displayed on a different monitor.

Project Manager - Multiple projects in a single pane

Multiple projects opened in the same session are displayed as docked and tabbed panes in a single Project Manager window.

This is different from previous releases, where a different Project Manager window opened for each project.
In addition, each project displays folders for the following additional resources:

- Layout
- Outputs
- PSpice Resources
- Logs
Common Window for Component Placement

In Capture, you can add components using the Place Part, PSpice Part Search, or Modeling Application. Starting with this release, these panes open in a single window. If multiple panes are opened, they are docked and arranged as tabs as shown in the following figure.

Common Window to Display Output

A common window is the area in the Capture workspace that allows you to view any kind of output: results, messages, errors, or warnings. This output is displayed in various panes, which are docked and tabbed as shown in the following figure:
Cadence Allegro and OrCAD Products: What's New in Release 17.4-2019
OrCAD Capture and OrCAD Capture CIS

- DRCs
- Online DRCs
- Command Window
- Session Log
You can access all the output panes from the View menu.
Single-Point Access to Modeling Applications

You can now access and use modeling applications from a single pane. To open the `Modeling Application` pane, click the Modeling Application icon ( ) in the `PSpice` toolbar or select `Place – PSpice Component – Modeling Application`. This is different from previous releases where the various modeling applications were part of an extended menu as shown in the following figure.
Enhanced Search Pane

The Find command is now available as a separate pane, called the Find pane. It allows you to specify a property value string and lets you select the object that you want to find. Capture then searches for all objects that match the specified string.
Simplified and Improved PCB Design Flow

After creating a schematic and verifying the logic by simulating the design in PSpice, generating the physical layout used to be a multi-step process in previous releases.

In 17.4-2019, creating the physical layout is a one-step process. The Online DRC feature ensures that all checks are done in real time as you create your schematic. The Online DRC checks are also performed as soon as you open a schematic. After your schematic is complete, all you need to do is access the new PCB menu and select the New Layout option. In addition, this release offers the following enhancements in the PCB design flow:

- Online DRC
- PCB Menu
- New Layout Window
- Design Sync
- Design Sync Setup

Online DRC

The enhanced user interface of Design Rules Check introduces a new option—Online DRC. Set this to On if you want to check and list design rule violations dynamically as you create or update a schematic design.

The Design Rules Check window enables you to set the rules to be run in Batch and/or Online mode.
In the output pane, you can see a new window—*Online DRCs*. It allows you to view the DRC checks in real time.
PCB Menu

All the tasks required for physical layout creation are now listed under a new menu—*PCB*. Using this menu, you can:

- Create a new layout.
- Synchronize design changes and execute ECOs.
- Launch Constraint Manager.
- Manage DRCs.
- View reports.
- Set power nets.
New Layout Window

Create a physical layout using a simplified user interface, *New Layout*, without having to separately create a PCB netlist.

![New Layout Window](image)

*Layout Folder in Project Manager*

To access the layout associated with a project, a new folder is introduced in Project Manager—*Layout*. 
Double-click the layout file associated with a project to open it. To add a new layout file, right-click the **Layout** folder and select **Add Layout**.
**Design Sync**

To efficiently and easily synchronize changes from schematic to layout, and from layout to schematic, a new user interface, *Design Sync*, has been introduced in 17.4-2019.

Using the *Design Sync* window, you can view the differences between a schematic and the layout for a board, and synchronize the layout from schematic or schematic from layout.

Designed with the capability for in-memory synchronization, you can use Design Sync to review the type of change, addition, modification, or removal of a design object without saving the design/layout.

To use this function, click the *Launch Design Sync* icon ( ) from the PCB toolbar, select *PCB – Design Sync*, or right-click the board file under the *Layout* folder in the project manager and select *Design Sync*.

![Design Sync Window](image)

The *Schematic* and *Layout* drop-down lists display the location of the project and board files respectively. If there are multiple board files, click the drop-down list to select the required board file. Click to change the direction of the arrow.

When you click this button, you can view connectivity differences from:

- Schematic to Layout
- Layout to Schematic
The *Preview* section displays all the differences between a schematic and board based on the direction of the arrow:

- Change Type
- Object
- Action
- New Value
- Old Value

Next, click the *Sync* button. If the arrow is from Schematic to Layout, changes are annotated from Capture to PCB Editor. If the arrow is from Layout to Schematic, changes in the PCB Editor board are backannotated to the Capture schematic to ensure that the physical board design is consistent with the logical schematic design.

**Design Sync Setup**

If you want to specify any additional options before creating the physical layout, such as a specific layout tool to be used or ECO options, use the *Design Sync Setup* window.
Introduced in 17.4-2019, use this dialog box to specify advanced PCB design flow settings in a single and separate window. To access this window, select PCB – Design Sync Setup.
Accessing External Parts from Capture

Using the Place – Search Providers menu, you can search for and download millions of electronic components, symbols, footprints, manufacturer datasheets, and 3D STEP models from Cadence-supported content providers — SamacSys and Ultra Librarian. You can easily find the part you require and place it in your design. The part, its associated metadata, and any available ECAD models, are saved to your local library.

Using a familiar web-based search experience, search for component data based on electrical parameters, as well as supply chain information, such as cost and availability. You can also further filter the results to narrow in on the component you need.

For details on the Search Providers feature, see Unified Search Quick Start Guide.
New Capture Start Page

In 17.4-2019, OrCAD Capture Start Page has a new look and feel, and its appearance aligns with the application theme.
PSpice and PSpice Advanced Analysis

This section describes the following enhancements and new features in PSpice and PSpice Advanced Analysis in release 17.4-2019.

- **Enhancements in PSpice Workspace** on page 79
  - Application Theme
  - Streamlined Workspace

- **New PSpice Models and Library** on page 87

- **PSpice Library Cleanup** on page 87
Enhancements in PSpice Workspace

The following new improvements have been done in the PSpice and PSpice Advanced Analysis workspace to ensure greater ease of use and satisfactory user experience.

- **Application Theme**
- **Streamlined Workspace**
Application Theme

In 17.4-2019, both PSpice and PSpice Advanced Analysis open in a dark theme. A dark theme reduces power usage, improves visibility, and makes it easier for screens to be read.

*PSpice in Dark Theme*
PSpice Advanced Analysis in Dark Theme
Setting Application Theme

To set the desired theme, select `Tools – Options`. In the `Probe Settings` window, click the `Color Settings` tab to select a Dark or Light application theme. The theme set in this window is also propagated to PSpice Advanced Analysis and Model Editor.
Streamlined Workspace

Panes are now displayed consistently across all OrCAD applications. All resources open as horizontal Tabbed Documents. By default, all panes displaying any kind of output are at the bottom of the application. If multiple panes are open in the output window, they are displayed as docked and tabbed panes as shown in the following figure.

In PSpice, the output window shows the following panes:

- Simulation Status
Customizing Panes

You can drag and drop panes to move them in the workspace using docking markers as shown in the following figure.
Alternatively, you can use the pop-up menu options available for each pane, such as *Floating*, *Docking*, and *Tabbed Document*. 
Multiple Monitor Display

You can drag a tabbed document and display it on another monitor as shown in the following figure. In this example, an active trace has been dragged and it becomes a separate window that can be displayed on a different monitor.
New PSpice Models and Library

Gallium nitride devices are increasingly used in the power engineering world. To support these kinds of devices, a new PSpice library, Transphorm_GaN.lib, comprising high-performance and high-reliability GaN MOSFET models, has been introduced in 17.4-2019.

Here is the list of GaN MOSFET models added to Transphorm_GaN.lib:

- TP65H035
- TP65H050
- TPH3202
- TPH3205B
- TPH3206
- TPH3207
- TPH3208
- TPH3212

Further, a new PSpice model for TLE8110EE, a 10-channel low-side switch in Smart Power Technology (SPT) with Serial Peripheral Interface (SPI) and 10 open-drain DMOS output stages, has been added to the PSpice library. This model is in the special_purpose_ics.lib PSpice library.

PSpice Library Cleanup

In 17.4-2019, the PSpice libraries have been reviewed and updated to fix bugs, such as inconsistent names, occasional use of invalid parameters, and syntax issues. Several duplicate models have also been removed.
Help System

Release 17.4-2019 has the following enhancements in the help system:

- Improved User Interface for Cadence Help on page 89
- Help Landing Page on page 90
- OrCAD Tutorial on page 92
Improved User Interface for Cadence Help

With 17.4-2019, the Cadence Help user interface has been enhanced for greater usability.

The elements of this new interface are explained in the following table.

<table>
<thead>
<tr>
<th>User Interface Element</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Click this icon to show or hide the <em>Library</em> pane.</td>
</tr>
<tr>
<td>2</td>
<td>Toolbar that allows you to browse between topics (Previous and Next), go to the welcome page, and search through documentation.</td>
</tr>
<tr>
<td>3</td>
<td>Breadcrumbs for each topic that support secondary navigation so that you do not have to open the <em>Library</em> pane.</td>
</tr>
<tr>
<td>4</td>
<td>Consolidated application menu that provides various options to use Cadence Help.</td>
</tr>
</tbody>
</table>

Chapter overview

This chapter provides introductory information to help you enter circuit designs that simulate properly. If you want an overview, use the Checklist for simulation setup to guide you to specific topics. Refer to the OrCAD Capture User Guide or Design Entry HDL User Guide for general design entry tool information.

Topics include:
- Checklist for simulation setup
- Using parts that you can simulate
- Using global parameters and expressions for values
- Defining power supplies
- Defining stimuli
- Things to watch for

Checklist for simulation setup

This section describes what you need to do to set up your circuit for simulation.

1. Find the topic that is of interest in the first column of any of these tables.
2. Go to the referenced section. For those sections that provide overviews, you will find references to more detailed discussions.
Help Landing Page

In 17.4-2019, when you open Cadence Help from your product using Help – Documentation, a new landing page appears as shown in the following figure. It has three main sections—What’s New, Featured Content, and Knowledge Support.
OrCAD Tutorial

Starting with this release, a design sample-based tutorial has been introduced in the OrCAD documentation set. This tutorial uses a fan-control module that you can use to run through the basic tasks in the PCB design process: schematic design creation, simulation, and board layout creation. You can access this tutorial from Help – Documentation of OrCAD Capture. Point the cursor to What’s New and click OrCAD Tutorial.